16 Channel High Voltage Board

Hardware Design and Test Document

Revision History

Date	Revision	Author	Comment
July 15, 2003	New	Fred Keske	Initial Release
August 8, 2003	A	Fred Keske	Cleaned-up test procedures
August 22, 2003	B	Fred Keske	Added Table 3
November 7, 2003	C	Fred Keske	Fixed typo in 2.1.2, item 2

1 High Voltage Functional Overview

The High Voltage Board is comprised of 16 channels that can swing +/- 450 volts that is used to drive piezo material as part of an Adaptive Optics System. Each channel is individually addressable through one of two Digital to Analog Converters (DAC) on board. Dipswitches set the upper three address bits for the board.

1.1 Functional Requirements

The following is a list of guidelines and requirements for the High Voltage Board design:

- Load = 9nF (mirror segment) + 300pF (cabling) = 9.3nF
- Output voltage range = ±450 volts
- 250 volt maximum swing for an update period (T0)
- Update period (T0) = $1/10^{th}$ of 2kHz = 50µs
- Slew rate = 250V/50µS = 5V/µs

1.2 Electrical Characteristics

A block diagram showing the implementation of the High Voltage Board is shown below in Figure 1.

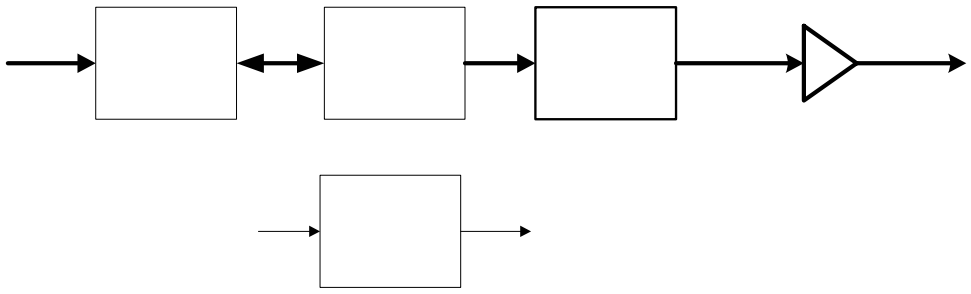


Figure 1

1.2.1 Input Power

The High Voltage Board is designed to operate from +5VDC ±5%, 21mA typical operating current.

1.2.2 Power Supply

The power supply block provides the -5 volts to the DACs. This function is performed with a MAX 764 which is an inverting switching regulator using a 5 volt input. The part requires a maximum of supply current of 120uA and will provide a minimum output current of 150mA @ -5 volts.

1.2.3 Bus Control

Control of the interfaces to the VME backplane and to the Digital to Analog Converter (DAC) is with a Cypress CPLD (CY37256). This part controls the bus transceivers (74ACTQ245) which provides the address (ADDR[0..7]), data (D[0..15]), and control

(CTRL[0..15])to the transceivers which in turn controls the data from the VME backplane. The CPLD also provides the data (DO[0..12]) and control to the two DACs.

Shown below is the board address range select:

Switch			Address Range
5	6	7	
ON	ON	ON	**0-11**
OFF	ON	ON	**12-23**
ON	OFF	ON	**24-35**
OFF	OFF	ON	**36-47**
ON	ON	OFF	**48-59**
OFF	ON	OFF	**60-71**
ON	OFF	OFF	**72-83**
OFF	OFF	OFF	**84-95**

Table 1

Note: switches 1 through 4 and 8 are not used and should remain in the '**ON**' position.

1.2.4 Digital to Analog Converter

The Digital to Analog (DAC) function is performed with two 13-bit DACs (MAX547). Each of these DACs provides eight channels to the high voltage amplifiers. The digital data interface is offset binary in which 0 to 8191 is scaled to the -4.5V to +4.5V output respectively.

1.2.5 High Voltage Amplifiers

A high voltage amplifier (PA95) that can swing from -450V to +450V is used to drive the piezo material. The gain is set to 99 to amplify the -4.5V to +4.5V input signal originating from the DAC.

1.2.5.1 Current Limit

The current limit is set to 45.7mA with the three-5.11Ω resistors in series. The limit value is derived from using a 1.7A Sorensen power supply driving the higher capacitive 24 outer actuators with a 0.6 de-rating factor.

1.2.5.2 Loop Stability

C47, R27, and C48 have been added to ensure loop stability. In addition, three 3.3Ω resistors in series have been added to the output of the amplifier to isolate the load somewhat.

As can be seen by the Bode Plot in figure 2, we have a good rate of closure of 20dB/decade. The phase shift plot shown in figure 3 indicates a good phase margin of 45°.

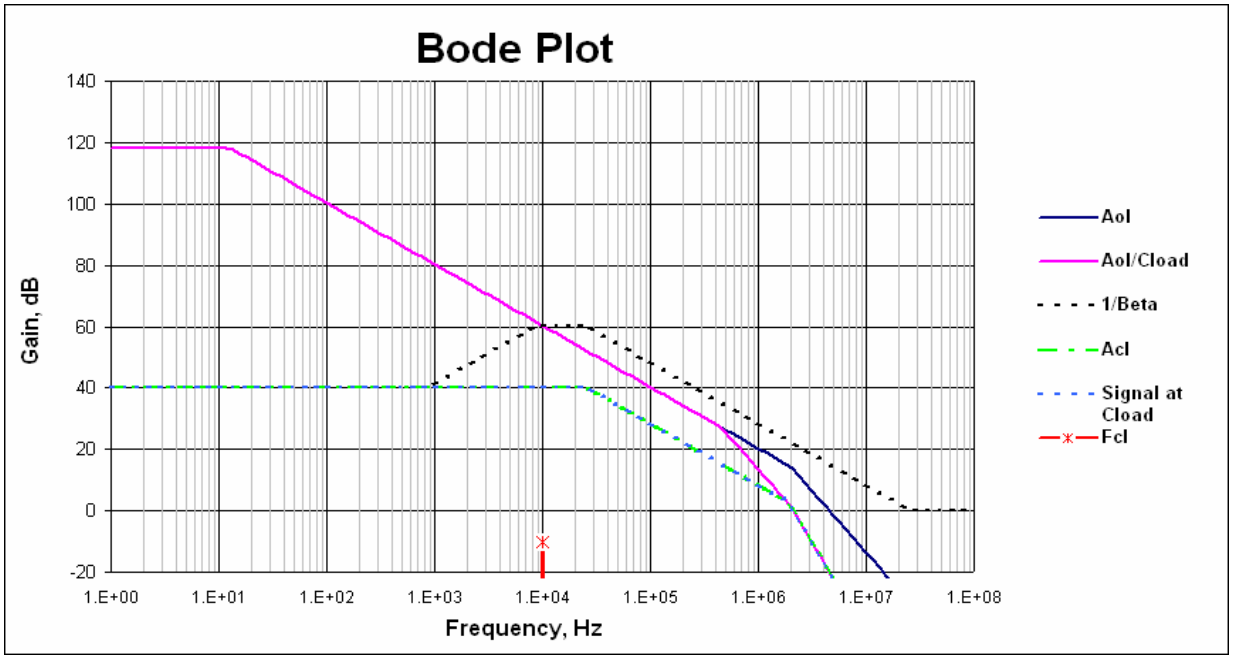


Figure 2

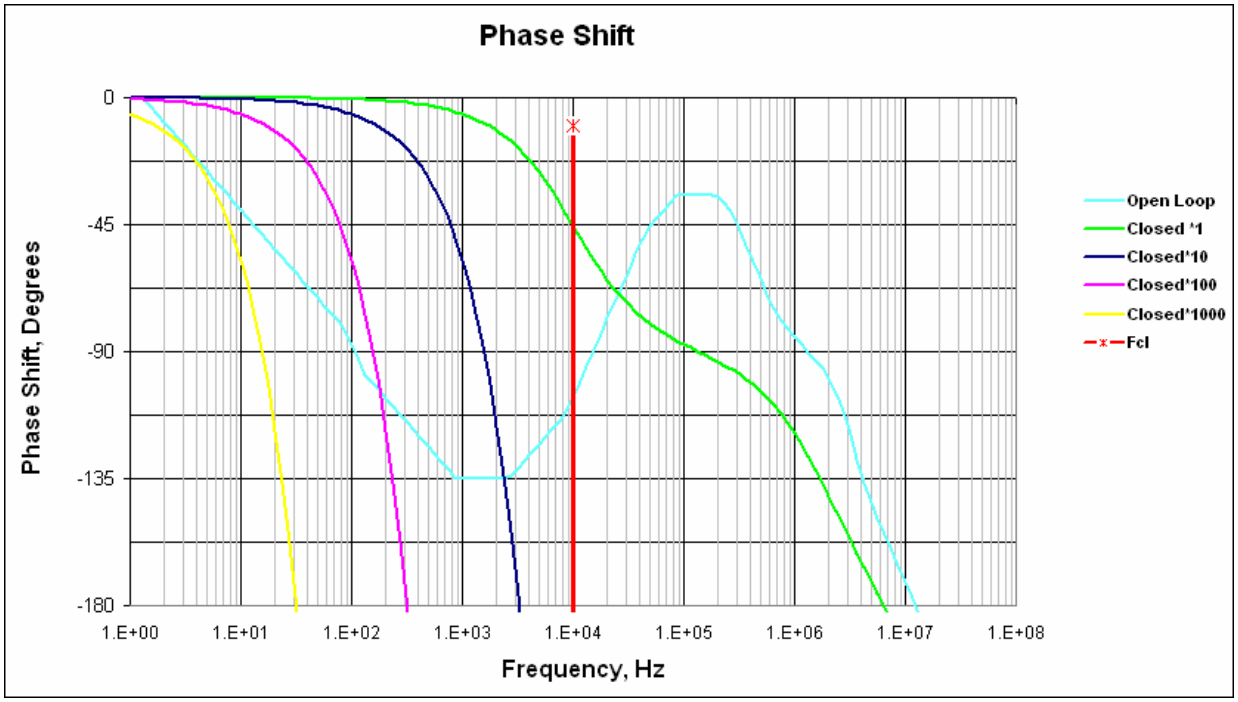


Figure 3

1.2.5.3 Slew Rate

The slew rate is based on the maximum current the amplifier is able to source, which in this case is determined by the current limit resistor and the total capacitance of the load. 45.6mA/9.3nF = 4.9V/μs.

1.3 Board Connections

1.3.1 Edge connectors

1.3.1.1 Backplane Connector

The Backplane connector labeled P1 is used to connect the High Voltage Board to the VME backplane. The signals available on the connector are: R_CTRL[0..6,8,10,11,13] used for control, RB_D[0..13] used for data, and R_ADDR[0..7] used for address.

1.3.1.2 High Voltage Connector

The High Voltage Connector is used to connect the High Voltage Board to the piezo element material. Pin 1 is located on the right side of the connector. The connector encompasses the original 12 channels on the top and bottom rows along with the addition of the four new channels on the middle row. See sheet 1 of the schematic for connection details and also the .

1.3.2 Headers

1.3.2.1 JTAG Header

The 10-pin JTAG header designated as JP1 is used to program the CPLD.

1.3.2.2 Test/Debug Header

JP2 is a 10-pin header that is used as a test and debug connector for the CPLD which is not used in normal operation. Pin 1 is located at the bottom left corner of the header.

1.3.2.3 VCC Header

JP3 is used to connect +5 volts to the board. Pin 1 is located at the top of the header. See Pin-out below.

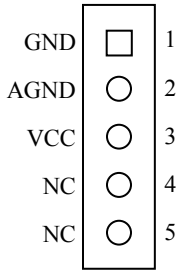


Figure 4

1.3.2.4 High Voltage Header

JP4 is used to connect ±350 volts to the board. Pin 1 is located at the top of the header. See Pin-out below.

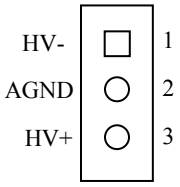


Figure 5

1.3.2.5 Channel Header

There is a 3-pin header for each of the 16 channels. The header is designated as JP5 with an appended alpha character specifying the respective channel. Pin 1 is the Analog ground, pin 2 is to monitor the output of the DAC, and pin 3 is to drive the input of the power amplifier with a ±4.5 volt signal. Pin 1 is located at the left side of the header. See Pin-out below.

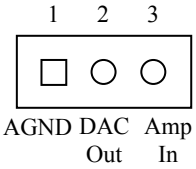


Figure 6

1.4 Channel Sequence

The High Voltage Board was designed with an additional four channels over the previous version of the board for a total of 16 channels that are now available to the backplane. The table below lists the board channel designation, the on-board circuit components designated with an alpha subscript, and the backplane channel designation, which also corresponds to the present software.

Board Channel Sequence	Channel Component Subscript	Backplane Channel Sequence
1	A	0
2	B	1
3	C	2
4	D	3
5	E	4
6	F	5
7	G	N/A

8	H	N/A
9	I	6
10	J	7
11	K	8
12	L	9
13	M	10
14	N	11
15	O	N/A
16	P	N/A

Table 2

1.4.1 Board to DM Connections

The table below lists the board channel pin to MS27467T19 connector pin to the pad number on the DM.

Backplane Channel	P2A Board Pin	MS27467T19 Pin	System Channel	DM Pad
0	Z26	46	HV36	17
1	D24	47	HV37	18
2	Z22	48	HV38	34
3	D20	49	HV39	35
4	Z18	51	HV40	55
5	D16	52	HV41	56
6	Z14	53	HV42	81
7	D12	54	HV43	82
8	Z10	56	HV44	83
9	D8	57	HV45	84
10	Z6	58	HV46	85
11	D4	59	HV47	86

Table 3

2 Test Procedure

Shown in the figure below is the top side of the board. The headers that are used in testing with its associated pin 1 are designated.

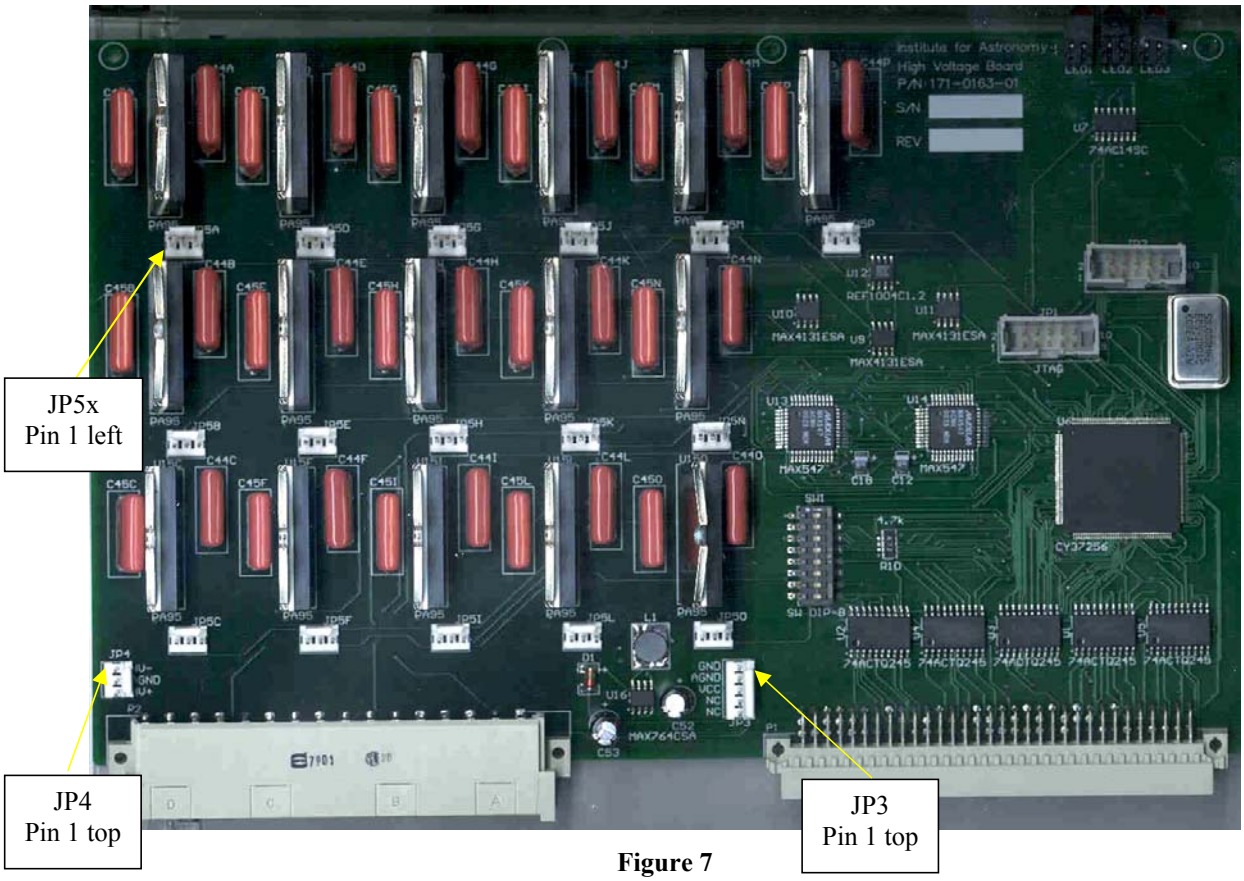


Figure 7

2.1 High Voltage Amplifier Channel Low Voltage Bench Test

2.1.1 Test Requirements

- Function Generator
- Oscilloscope, 2 channel
- DC Power Supply with 15V and -15V outputs
- Cables to connect power supply and Function Generator to board

2.1.2 Procedure

1. Set up the function generator to create a square wave with a 4ms period and amplitude +/-100mV.
2. On **JP4,** connect -15V to pin 1, GND to pin 2, and +15V to pin 3.
3. Turn on the power supply.
4. On **JP5A,** connect output of the Function Generator to pin 3 and GND from the Function Generator to pin 1.
5. Also, connect the output and GND from the Function Generator to channel A of the oscilloscope. Set the channel to 50mVDC and 1ms.
6. On **P2**, connect the second channel of the oscilloscope to pin z26 on the high voltage connector using an appropriate breakout connecter. Set the channel to 5VDC
7. Check to see that:

a. The waveform on channel B of the oscilloscope swings from -10V to +10V.
b. The waveform on channel B of the oscilloscope is approximately 180° out of phase when compared to channel A of the oscilloscope.
c. The transitions are fast and not rounded at the top.

8. If any of the above criteria are not met, the channel fails the test. Keep track of board serial number and channel for debugging.
9. Repeat steps 5-8 using corresponding connector in step 5 for each of the channels.
10. If all channels pass testing, board has passed *High Voltage Amplifier Channel Low Voltage Bench Test.*

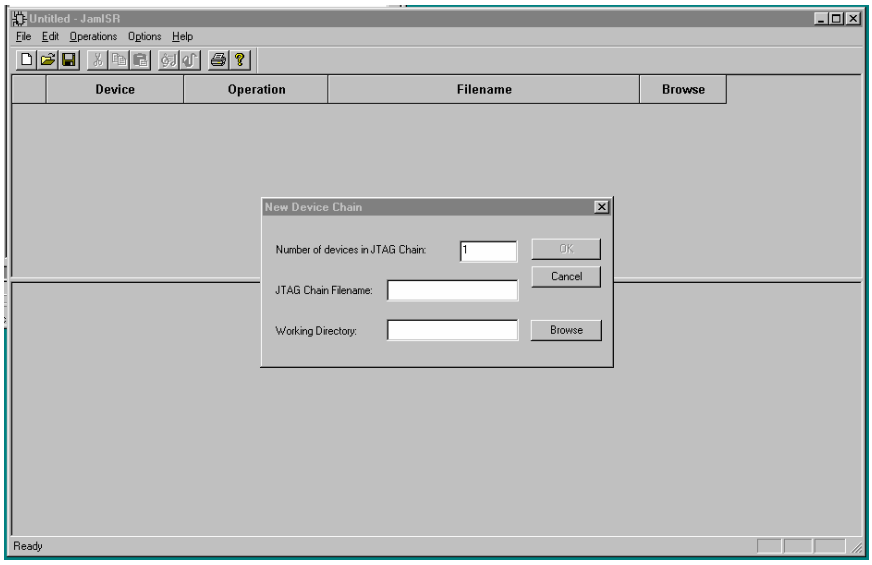
2.2 CPLD Programming

2.2.1 Requirements

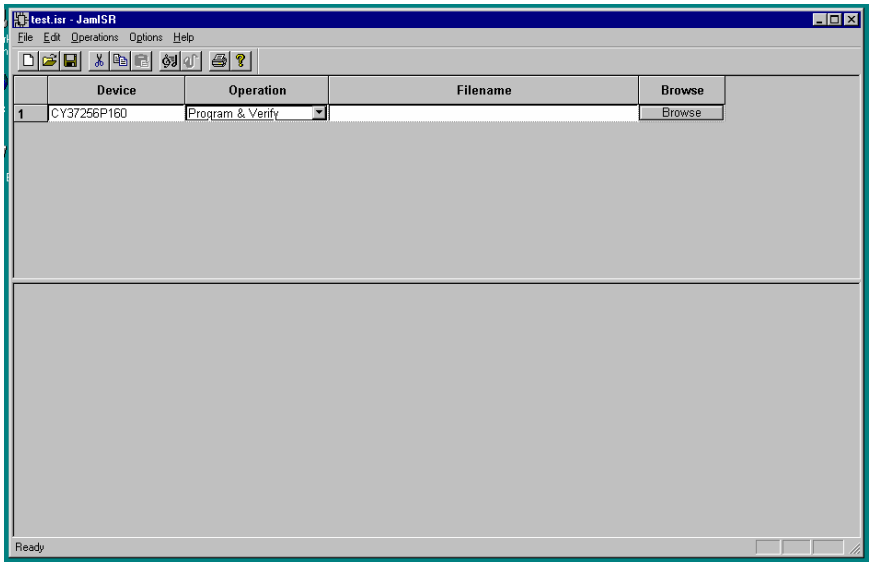
- Cypress ISR programming software
- Cypress UltraISR programming cable
- 5V power supply
- hva.jed programming file

2.2.2 Procedure

1. Plug Cypress UltraISR programming cable into the parallel port of the PC and start the Cypress ISR programming software.
2. Select '**New**' from the '**File**' menu



3. Type '**1**' in the '**Number of devices in JTAG Chain**' text box.
4. Type any filename in the '**JTAG Chain Filename**' text box.
5. Browse and select or type in the directory that you would like to save the programming session.
6. Press '**Ok**'



7. In the 'Devices' box select '**CY37256P160**'.
8. In the '**Operation**' box, select '**Program & Verify**'.
9. Use the '**Browse**' button to locate and set the path and filename in the '**filename**' text box to 'G:\\Electronics\arc_2001_1_17\vhdl\HVA\hva.jed.
10. Press the  button to compose the programming file.
11. On **JP3,** connect power supply GND to pins 1 and 2, +5V to pin 3.
12. Connect Cypress UltraISR programming cable to header **JP1**. Connector should be polarized, but if not ensure that pin 1 of cable connects to pin 1 of the header.
13. Turn on the power supply.
14. Press the  button to program the CPLD. Programming may take several second to complete
15. Check the log that is displayed to see that the CPLD programmed and verified successfully.
16. If programming or verify was not successful:
    a. Verify that the path and filename are correct in the '**filename**' textbox. If not, repeat from step 9.
    b. Check to see that power and ground are connected correctly and that supply voltage is set to 5VDC. If not, repeat form step 11.
    c. Check to see that part is installed and soldered correctly to board. If not, correct problem and repeat from step 11.
17. Turn off power supply and disconnect cables.

2.3 DAC Address Test

2.3.1 Requirements

- 2 Multifunction Boards
- 1 Chassis
- 2 PCs with Linux OS
- 2 FC-FC Multimode Fiber Optic Cables

- Oscilloscope

2.3.2 Procedure

1. If not already done so, log into AOUIM by typing '**ao**' and hitting return.
2. Type the password, '**wai!mea**' and hit return.
3. Start xwindows by typing '**startx**'
4. On AOUIM, open 3 Xterm windows
5. In first Xterm window type '**rlogin –l ao aoicm**' and hit return.
6. Type the password, '**wai!mea**' and hit return.
7. Change to the '**manoa85/dio32**' directory.
8. Type '**su aroot**' and hit return.
9. Type the password, '**wai!mea**' and hit return.
10. Type '**start_dio**' and hit return. This should start dio32.
11. In second Xterm window type '**rlogin –l ao aoicm**' and hit return.
12. Type the password, '**wai!mea**', and hit return.
13. Change to the '**manoa85/dio32**' directory.
14. Type '**cat /dev/rtf0**' and hit return.
15. In the third Xterm window, type '**rlogin –l ao aoicm**' and hit return.
16. Type the password, '**wai!mea**' and hit return.
17. Change to the '**manoa85/dio32**' directory.
18. Type '**cat > /dev/rtf1**' and hit return.
19. You should now be able to see the commands that you type in Xterm 3 show up in Xterm window 2. To test this, type '**test**' in Xterm 3. If you do not see '**test**' in Xterm 2:
    a. Hit '**ctrl-c**' in Xterm 3.
    b. In Xterm 3, type '**exit**' and hit return.
    c. Hit '**ctrl-c**' in Xterm 2.
    d. In Xterm 2, type '**exit**' and hit return.
    e. In Xterm 1, type '**stop_dio**' and hit return.
    f. Repeat from step 7.
20. Make sure that all dip switches on SW1 are in the '**ON**' position
21. Plug board that into the chassis.
22. On **JP5A**, connect oscilloscope GND to pin 1 and oscilloscope channel A to pin 2. Set the voltage scale to 5VDC with the time base at 20ms/division.
23. Turn on power by flipping switch on front of chassis
24. In window #3, type '**a i**' and hit return.
25. Type '**f m 1**' and hit return to set the test pattern to saw tooth.
26. Type '**f p 10000**' and hit return to set the period of the pulse to 80 ms.
27. Type '**f a 0**' and hit return to direct commands to HV0.
28. Type '**f b**' and hit return to start pattern generation.
29. Check the oscilloscope to see a saw tooth pattern is being generated. If output stays constant on oscilloscope:
    a. Turn off chassis power by flipping switch on front of chassis.
    b. Wait 5-10 seconds and turn power back on.
    c. Check if pattern is being generated.

d. If still no output, move oscilloscope probe to corresponding connector on channel A and type '**f a 1**' and hit return, then repeat steps 21through 24.
e. If not, repeat the above steps **a** through **c** four times.
f. If still no output, there may be a problem with one of the DACs. Turn off chassis and remove board. Check for assembly errors around U13 and U14.

30. Move switch #5 on SW1 to the 'OFF' position.
31. Type 'f a 12' and hit return.
32. Type 'f b' and hit return.
33. Check oscilloscope to make sure that the saw tooth pattern is being generated.
34. Type 'f a 1' and hit return.
35. Check to make sure that the saw tooth pattern is NOT being generated.
36. Type 'f a 24' and hit return.
37. Check to make sure that the saw tooth pattern is NOT being generated.
38. Move switch #5 on SW1 to the 'ON' position and switch #6 on SW1 to the 'OFF' position.
39. Check oscilloscope to make sure that the saw tooth pattern is being generated.
40. Type 'f a 0' and hit return.
41. Check to make sure that the saw tooth pattern is NOT being generated.
42. Type 'f a 12' and hit return.
43. Check to make sure that the saw tooth pattern is NOT being generated.
44. Turn off power.

2.4 High Voltage Amplifier Test

2.4.1 Requirements

- Multifunction Boards
- 1 Chassis
- 2 PCs with Linux OS
- 2 FC-FC Multimode Fiber Optic Cables
- High Voltage Oscilloscope, 2 channel
- High Voltage Cable
- Piezo Material with two leads connected to it

NOTE: You will be working with +/-450 volts with this test. Make sure to follow **all** the steps in the order that they are written. Failure to do so could result in serious electrical shock.

2.4.2 Procedure

2.4.2.1 High Voltage Test

1. If not already done so, perform steps 1 through 21 from section 2.3.2.1 to enable the test program.
2. On **JP5A**, connect oscilloscope GND to pin 1 and oscilloscope channel A to pin 2. Set the voltage scale to 5VDC with the time base at 20ms/division.
3. Turn on power by flipping switch on front of chassis

4. In window #3, type '**a i**' and hit return.
5. Type '**f m 1**' and hit return to set the test pattern to saw tooth.
6. Type '**f p 10000**' and hit return to set the period of the pulse to 80ms.
7. Type '**f a 0**' and hit return to direct commands to HV0.
8. Type '**f b**' and hit return to start pattern generation.
9. Check the oscilloscope to see a saw tooth pattern is being generated. If output stays constant on the oscilloscope:
    a. Turn off chassis power by flipping the switch on the front of the chassis.
    b. Wait 5-10 seconds and turn power back on.
    c. Check if pattern is being generated.
    d. If not, repeat the above steps **a** through **c** four times.
10. Install the high voltage connector assembly in the J2 connector on the PCB.
11. Insert the 12 individual shrink-wrapped pins into the PCB side of the high voltage connector corresponding to the 12 channel pins inside the connector.
12. Connect the high voltage supply to **JP4**.
13. Turn on the high voltage power supply from the power strip. Make sure the voltage is at 450 volts on both supplies.
14. Connect probe of channel B on the oscilloscope to the shrink-wrapped pin corresponding to high voltage channel 0. Set the voltage scale to 200VDC.
15. Check to see that the voltage from oscilloscope channel B roughly follows the saw tooth pattern on oscilloscope channel A and that the voltage is approximately +/-450V.
16. Turn off the high voltage power supply from the power strip
    NOTE: This is a very important step as +/-450V is being carried on the high voltage cable. If you do not turn off the high voltage supply before doing this step, there is a high risk for electrical shock.
17. Type '**f a 6**' and hit return to direct commands to HV6.
18. Check that the channel being tested is NOT outputting the saw tooth pattern (unless HV6 is the channel being tested, which is on **JP5I**). If output remains flat, channel has passed the test.
19. Move oscilloscope channel A probe to the corresponding **JP5** connector on the next channel with the oscilloscope channel B probe to the corresponding socket on the high voltage cable.
20. Turn on the high voltage power supply from the power strip.
21. Type '**f a 0**' and hit return to direct commands to HV0.
22. Check that the channel is NOT outputting the saw tooth pattern. If output remains flat, channel has passed the test.
23. Type '**f a x**' with '**x**' being the corresponding channel number that is being tested, then hit return.
24. Check the oscilloscope to see a saw tooth pattern is being generated.
25. Repeat steps 13 through 24 until all the channels have all been tested, noting the pass/fail status of the channels.
26. Turn off all power supplies.
27. If not planning to test another board:
    a. Press 'ctrl-c' in Xterm 3.
    b. Type '**exit**' in Xterm 3 and hit return.

c. Press '**ctrl-c**' in Xterm 2.
d. Type '**exit**' in Xterm 2 and hit return.
e. In Xterm 1 type '**stop_dio**' and hit return.
f. Type '**exit**' and hit return.

2.4.2.2 Filter response test

1. Setup the function generator by setting the waveform to a square wave, the frequency to 2kHz, and the voltage to 0.35Vpp. Make sure the offset is set to zero.
2. Connect function generator probe to **JP5A** pin 3 and ground to pin 1. Set the voltage scale to 200mVDC with the time base at 50us/division.
3. Turn on the cursor data function dt and the dV on the oscilloscope.
4. Make sure the piezo material is **not** connected to the high voltage connector assembly. Turn on the high voltage power supply from the power strip. Adjust the voltage to 50 volts on both supplies.
5. Turn off the high voltage power supply from the power strip.
6. Connect the piezo material to the high voltage connector assembly.
7. Turn on the high voltage power supply from the power strip.
8. Connect probe of channel B on the oscilloscope element corresponding to high voltage channel 0. Set the voltage scale to 20VDC.
9. Place the vertical bar of cursor 1 on the oscilloscope on the edge of channel A and the horizontal bar of cursor 2 on the settled voltage of channel B.
10. Check to see that the dt value is less than 36us.
11. Move the horizontal bar of cursor 1 to the peak of channel B.
12. Check to see that the dV value is less than 7V.
13. Turn off the high voltage power supply from the power strip.
14. Move oscilloscope channel A probe to the corresponding **JP5** connector on the next channel with the oscilloscope channel B probe to the corresponding element on the piezo material.
15. Turn on the high voltage power supply from the power strip.
16. Connect probe of channel B on the oscilloscope element corresponding to the next high voltage channel.
17. Repeat steps 9 through 16 until all the channels have all been tested, noting the pass/fail status of the channels.
18. Turn off the high voltage power supply from the power strip.
19. Remove board from chassis.

Appendix A: Schematics

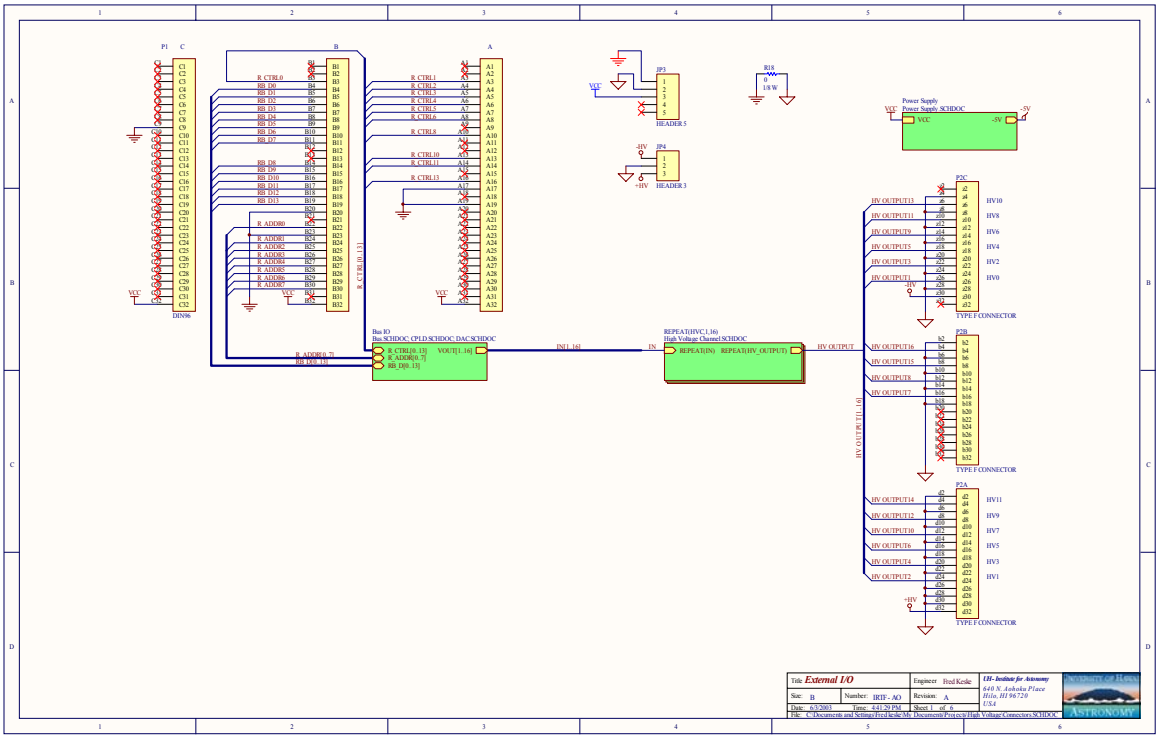


Figure 8

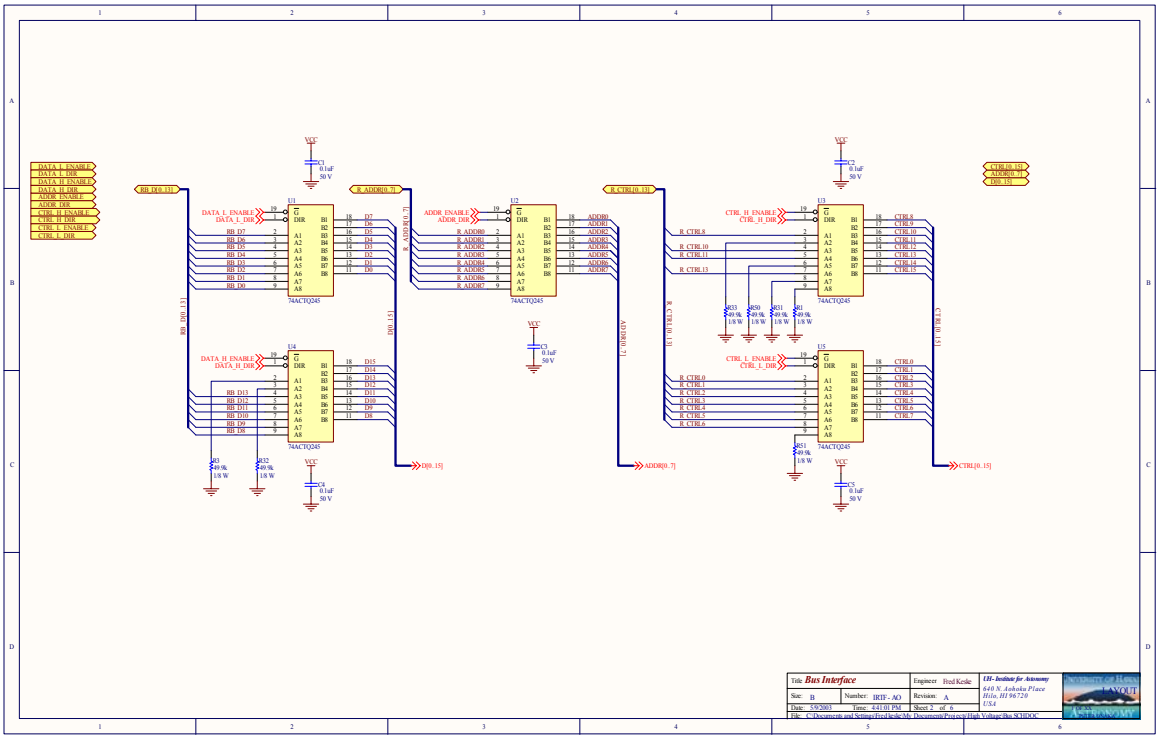


Figure 9

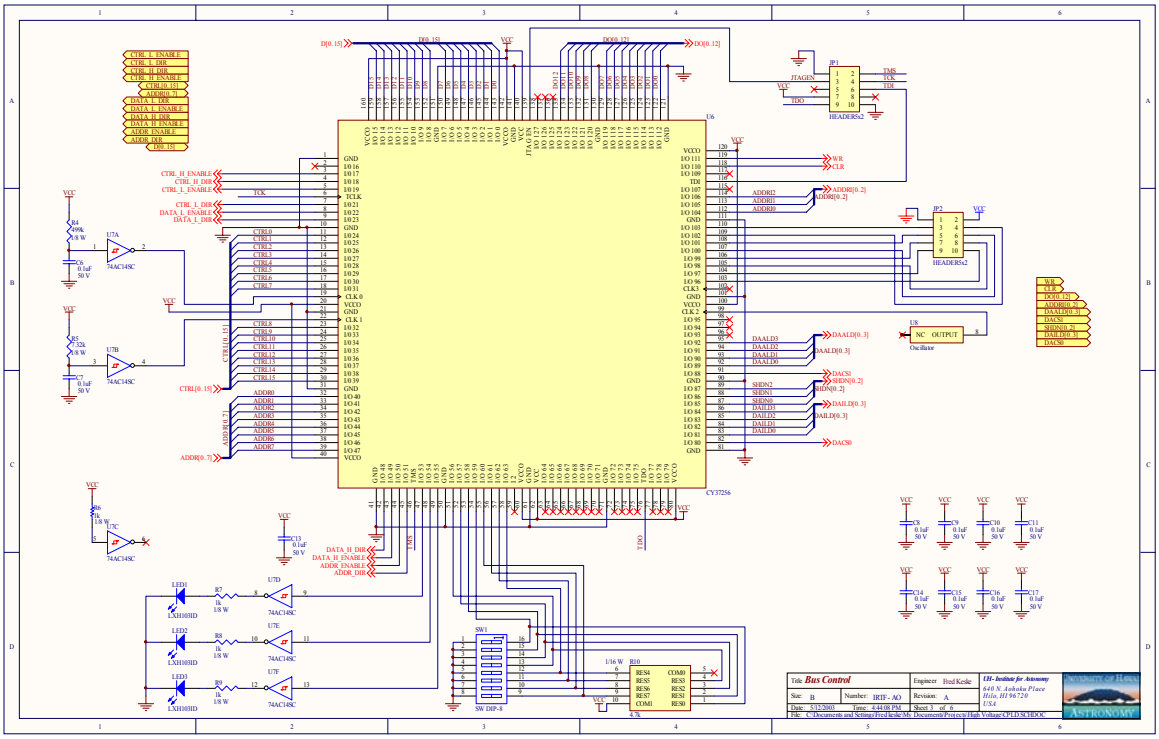


Figure 10

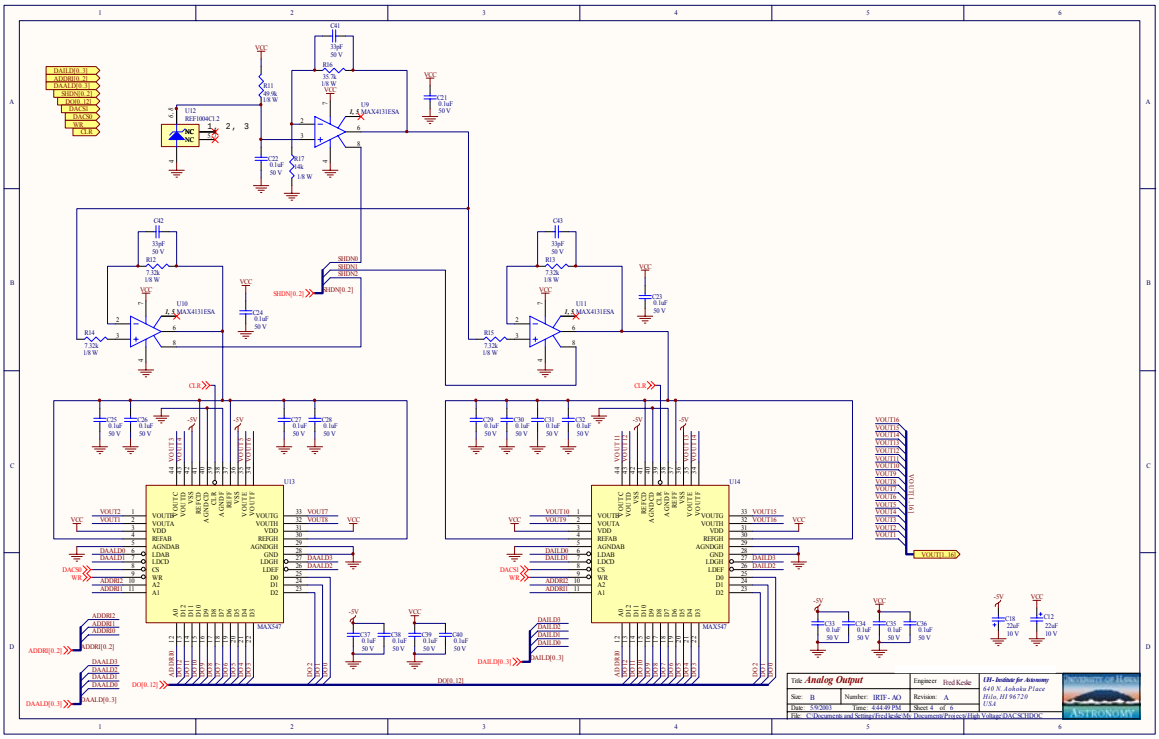


Figure 11

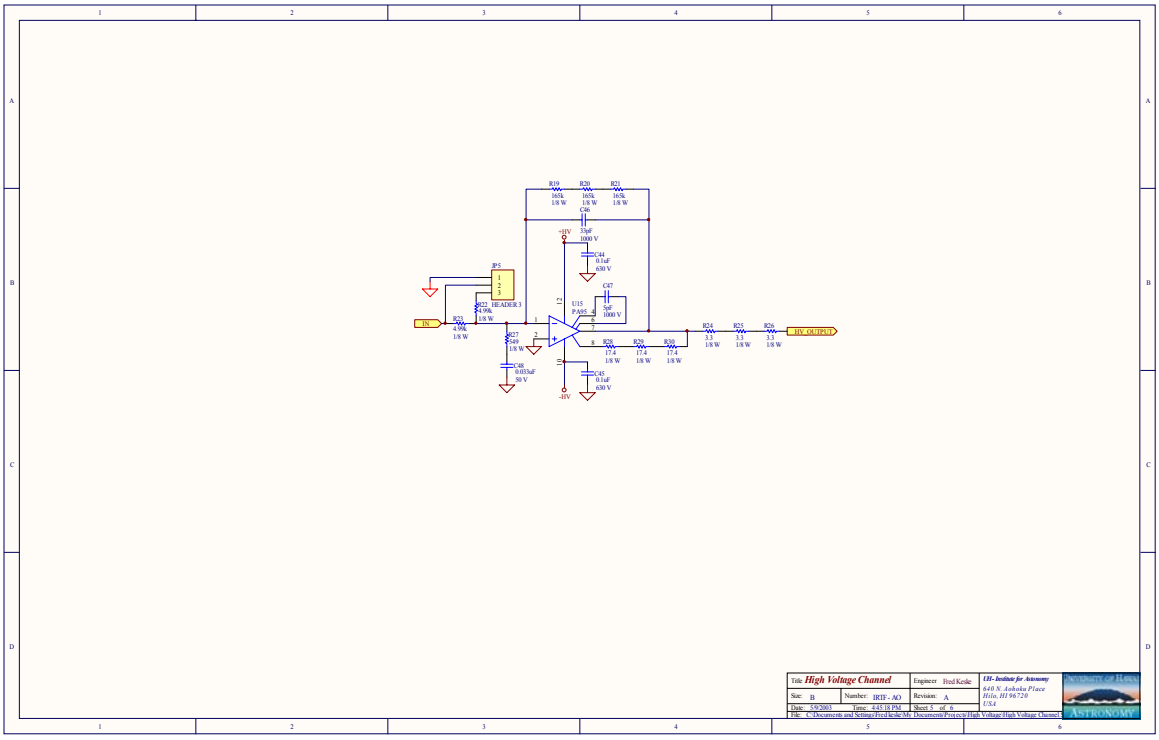


Figure 12

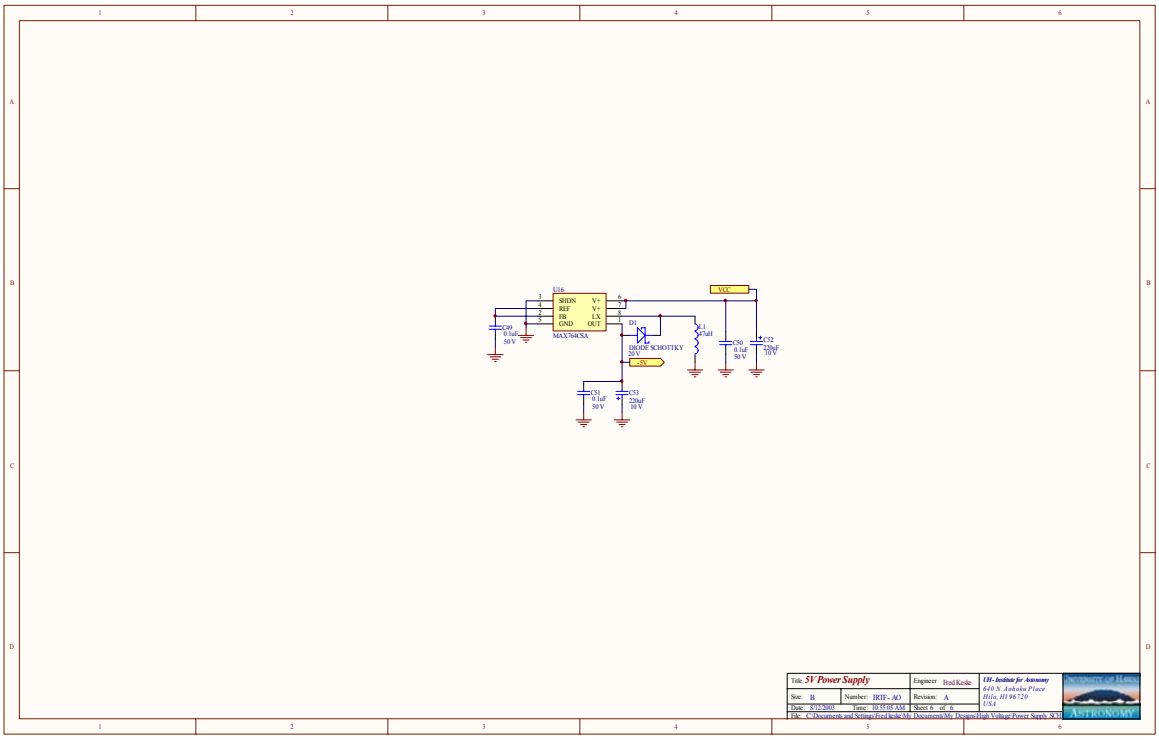


Figure 13